Optimizing An Innovative SAR Post-Processing Algorithm for Multi-Core Processors

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Optimizing SARMTI for Multi-Core Processors

• A major US defense contractor asked NA Software, Ltd*. and Intel’s Embedded Computing Division to multi-thread and evaluate an innovative SAR post-processing algorithm
  • “SARMTI” developed by Dr. Chris Oliver, CBE, of InfoSAR*
  • Identifies slow-/fast-moving targets from existing SAR data – no need for MTI radar

• Goals:
  • Phase 1: How will the original, serial algorithm scale across multiple processor cores when it is multi-threaded?
  • Phase 2: Can moving targets be detected, motions derived, and objects registered on a background SAR image in near real-time?
Existing SAR and MTI Algorithms

- **SAR**
  - Excellent along-track resolution -- \( \sim 1 \text{m} \)
  - Moving targets degrade result
- **MTI**
  - Poor along-track resolution \( >100 \text{m} \)
  - Good at identifying fast moving targets, but slow targets and ground clutter degrade result
  - Current “integrated” systems switch between SAR and MTI – require human analysis, several passes

*Existing SAR and MTI algorithms are both sub-optimal*
New SARMTI Algorithm from InfoSAR*

Existing SAR:
Moving targets are both shifted and blurred

After SARMTI applied to same SAR data: Targets detected (red circles) in correct positions within one SAR resolution cell

Corresponding motions are also derived

- Across-track acceleration and along-track velocity in addition to across-track velocity measured in typical MTI systems

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Multi-Threading: Round 1

- PPC code ported to IA
- Gnu* `gprof` used to determine time spent in each function ("hot spots")

<table>
<thead>
<tr>
<th>Time %</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.48</td>
<td>DETECTION.</td>
</tr>
<tr>
<td>53.07</td>
<td>FFTW Calls</td>
</tr>
<tr>
<td>11.22</td>
<td>OTHER COMPRESSION.</td>
</tr>
<tr>
<td>2.04</td>
<td>DATA EXTRACTION</td>
</tr>
<tr>
<td>96.81%</td>
<td>Total</td>
</tr>
</tbody>
</table>

- Multi-threaded compression and detection phases
- Restructured calls to most used target detection functions
  - Only a few calls—all in initial stage

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SARMTI: Multi-Threaded Structure

- Raw SAR image (>14MBytes) loaded into memory
- Serial processing for set-up, synchronization and image display
- Data tiles processed independently on each core (thread)
  - Avoid ‘cache thrash’: Be careful to use localized memory for each thread
  - Processor (Core) Affinity vs letting Linux dynamically place each process on least-loaded core
    - Load very balanced load either way. Went with Linux* for maximum portability
## Test Scenarios

<table>
<thead>
<tr>
<th>Test Scenario</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>run_sarmpi_test1</td>
<td>Uniform background with no targets</td>
</tr>
<tr>
<td>run_sarmpi_test2</td>
<td>Uniformed background with 10 moving targets</td>
</tr>
<tr>
<td>run_sarmpi_test3</td>
<td>Structured background with no targets</td>
</tr>
<tr>
<td>run_sarmpi_test4</td>
<td>Structured background with 10 moving targets</td>
</tr>
</tbody>
</table>
Compilers: Gnu vs Intel® C++ Compiler for Linux*

- gcc: Gave better results on FFTW* libraries
  - FFTW libraries developed and optimized using gcc

<table>
<thead>
<tr>
<th>Compiler Option</th>
<th>Scenario 1</th>
<th>Scenario 2</th>
<th>Scenario 3</th>
<th>Scenario 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SARMTI code = gcc  FFTW code = gcc</td>
<td>7.74 secs</td>
<td>9.9 secs</td>
<td>7.4 secs</td>
<td>13.9 secs</td>
</tr>
<tr>
<td>SARMTI code = icc  FFTW code = gcc</td>
<td>7.86 secs</td>
<td>10.1 secs</td>
<td>7.5 secs</td>
<td>14.1 secs</td>
</tr>
<tr>
<td>SARMTI code = icc  FFTW code = icc</td>
<td>10.25 secs</td>
<td>13.4 secs</td>
<td>9.7 secs</td>
<td>18.9 secs</td>
</tr>
<tr>
<td>SARMTI code = gcc  FFTW code = icc</td>
<td>9.75 secs</td>
<td>13.1 secs</td>
<td>9.3 secs</td>
<td>18.5 secs</td>
</tr>
</tbody>
</table>

- But overall SARMTI had very similar processing times with either compiler
Multi-Threading: Round 2

- ‘gprof’ rerun – remaining ‘hot spots’:
  - 54% FFTW Calls
  - 26% Target detection
  - 13% Data compression
  - 2.5% Data Extraction

- FFTW Library replaced by Intel® Math Kernel Library
  - Vector Math functions
  - “fftw wrappers”

<table>
<thead>
<tr>
<th>Scenario</th>
<th>1 (secs)</th>
<th>2 (secs)</th>
<th>3 (secs)</th>
<th>4 (secs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C vector code</td>
<td>6.9</td>
<td>9.3</td>
<td>6.9</td>
<td>12.8</td>
</tr>
<tr>
<td>MKL Vector</td>
<td>6.4</td>
<td>8.5</td>
<td>6.1</td>
<td>11.8</td>
</tr>
<tr>
<td>library time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MKL library</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>speed up</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MKL FFT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>speed up</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total MKL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>speed up</td>
<td>10.8%</td>
<td>6.1%</td>
<td>6.8%</td>
<td>7.9%</td>
</tr>
<tr>
<td></td>
<td>18.0%</td>
<td>14.7%</td>
<td>18.4%</td>
<td>15.7%</td>
</tr>
</tbody>
</table>

Note: Timings are for a 4x4C “Tigertown” processor system, but MKL speed-up percentages on “Dunnington” and “Nehalem” systems are similar.
Threaded Performance Speed-Up: 4x “Tigertown” Processor System
— 16 Physical Cores, 16 HW Threads per system

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Intel® Xeon® Processor</th>
<th>Serial Time (sec)</th>
<th>Threaded Time 16 Cores</th>
<th>Speed Up 0T→16T</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4x TGR</td>
<td>85</td>
<td>6.4</td>
<td>13.3X</td>
</tr>
<tr>
<td>2</td>
<td>4x TGR</td>
<td>120</td>
<td>8.5</td>
<td>14.1</td>
</tr>
<tr>
<td>3</td>
<td>4x TGR</td>
<td>104</td>
<td>6.1</td>
<td>17.0</td>
</tr>
<tr>
<td>4</td>
<td>4x TGR</td>
<td>166</td>
<td>11.8</td>
<td>14.1</td>
</tr>
</tbody>
</table>

Serial to 16-Thread Speed Up: 13-17X -- Approaches # of Cores

4x Intel® Xeon® L7345 Processors ("Tigertown") 4 Cores each @ 1.86 GHz each; 8MB L2 Shared Cache; 1 Thread/Core (See configuration information in Backup)
Threaded Performance Speed-Up: 4X
“Dunnington” Processor System
-- 24 physical cores, 24 HW Threads

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Intel® Xeon® Processor</th>
<th>Serial Time (sec)</th>
<th>Time (seconds) per Hardware Cores/Threads</th>
<th>Total Speed Up 0→24T</th>
<th>Speed Up 1→24T</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4x DUN</td>
<td>85.4</td>
<td>37.0 18.8 9.9 4.9 3.6 2.2</td>
<td>38.8X</td>
<td>16.8X</td>
</tr>
<tr>
<td>2</td>
<td>4x DUN</td>
<td>120.2</td>
<td>47.9 24.6 12.9 6.7 4.8 3.1</td>
<td>38.8X</td>
<td>15.5X</td>
</tr>
<tr>
<td>3</td>
<td>4x DUN</td>
<td>104</td>
<td>35.6 18.3 9.6 4.8 3.5 2.1</td>
<td>49.5X</td>
<td>17.0X</td>
</tr>
<tr>
<td>4</td>
<td>4x DUN</td>
<td>166.2</td>
<td>67.1 33.9 17.8 9.6 6.6 4.4</td>
<td>37.8X</td>
<td>15.3X</td>
</tr>
</tbody>
</table>

Single Threaded to Multi-Threaded Speed Up: 37-49X
1 Thread to 24 Thread Speed Up: 15-17X

4x Intel® Xeon® MP X7460 Processors (“Dunnington”) 6 Cores each @ 2.686 GHz, 16 MB Shared L2 Cache 1 Thread/Core (See configuration information in Backup)

Note that “Dunningtons” are pin-compatible with “Tigertowns”
Performance Scaling/Core: 4x 6 Core “Dunnington”

- Intel processors’ large L2 caches are a major factor in the high performance of this application/workload.
- Gain % slows > 8 threads, but is still significant overall.
  - Different portions of the algorithm use differently sized data sets, whose sizes change dynamically as the geometry changes. Some of the data sets do not thread as efficiently across 16 or 24 cores.
Threaded Performance Speed-Up: 2x “Nehalem” Processor System
– 8 Physical Cores, 16 HW Threads

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Intel® Xeon® Processor</th>
<th>Time (seconds) per Hardware Cores/Threads</th>
<th>Speed Up 1T→8 T</th>
<th>Speed Up 1T→16T</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2x NHL</td>
<td>29.04 15.28 7.87 4.77 4.26 4.19</td>
<td>6.1X</td>
<td>6.8X</td>
</tr>
<tr>
<td>2</td>
<td>2x NHL</td>
<td>36.93 19.29 10.04 6.31 5.4 5.61</td>
<td>5.8X</td>
<td>6.8X</td>
</tr>
<tr>
<td>3</td>
<td>2x NHL</td>
<td>27.95 14.69 7.57 4.43 4.03 4.16</td>
<td>6.3X</td>
<td>6.9X</td>
</tr>
<tr>
<td>4</td>
<td>2x NHL</td>
<td>53.5 27.45 14.15 7.5 7.4 7.73</td>
<td>7.1X</td>
<td>7.2X</td>
</tr>
</tbody>
</table>

1 Thread to 8 Thread Speed Up: 6-7X
Very Little Gain From Second HW Thread/Core
24 thread time worse because some cores are running > 2 threads

2x Intel® Xeon® DP X5570 Processors (“Nehalem-EP”) 4 Cores each @ 2.93 GHz, 2 Threads/Core (See Configuration information in Backup)
Threaded performance speed up: 2x 4 Core “Nehalem”

- Intel processors’ large L3 caches are a major factor in the high performance of this application/workload
- Some of the data sets do not thread efficiently across 16 or 24 cores. Timings for 24 threads are slightly higher because max HW threads on this system is 16
## Performance / SWAP Comparison

<table>
<thead>
<tr>
<th>CPU</th>
<th>Test 4 Time (seconds)</th>
<th>Processor Maximum Thermal Design Power</th>
<th>Deltas</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8T</td>
<td>16T</td>
<td>24T</td>
</tr>
<tr>
<td>Tigertown</td>
<td>11.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nehalem</td>
<td>7.5</td>
<td>7.4</td>
<td></td>
</tr>
<tr>
<td>Dunnington</td>
<td>9.6</td>
<td>6.6</td>
<td>4.4</td>
</tr>
<tr>
<td>Nehalem</td>
<td>7.5</td>
<td>7.4</td>
<td>7.73</td>
</tr>
<tr>
<td>Nehalem</td>
<td>4x</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4-socket Dunnington system: fastest overall time
Nehalem microarchitecture far more efficient core for core

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Phase 2 Study

- Offload FFTs and other parts of SARMTI to FPGA(s)
  - Xilinx* FPGAs/Nallatech* PCIe and In-Socket Accelerator Modules
  - Altera* FPGAs/XtremeData* In-Socket Accelerator Modules
- Demonstrate effectiveness of Intel® QuickAssist Acceleration Abstraction Layer (AAL)

Loosely Coupled FPGA accelerators -- PCIe

Tightly Coupled FPGA accelerators – Front Side (Processor) Bus

Results: <1s times achievable

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Intel® QuickAssist Acceleration Abstraction Layer

- Low level software runtime layer
- Service Oriented Architecture (SOA)
  - Publish/Request service model: database of acceleration functions
  - Virtualizes accelerators: multiple calls operate seamlessly
  - Implements system-wide resource aggregation and sharing policies
- Abstracts hardware details from application
  - Optimizes memory interaction between accelerators and operating system
  - Provides dynamic interface binding to acceleration packages
  - Dynamically reconfigures FPGAs
- Handles all types of accelerated workloads
  - Data parallel and/or task parallel
  - Asynchronous programming model: optimized for concurrent task processing
  - Very large to small data sets; streaming data
- Designed to be compatible with existing software development frameworks
AAL Conceptual Model

**Digital Signal Processing Application(s)**

**Domain Accelerator Libraries**
(Intel® Performance Primitives, FPGAlib, etc.)

**Acceleration Abstraction**
Service Layer

**WS0**  **WS1**  **WS2**  **WS3**  **WS4**

**AFU 0**  **AFU 1**  **AFU 2**  **AFU 3**  **AFU 4**
Accelerator Module 0  Accelerator Module 1  Accelerator Module 2  Accelerator Module 3  Accelerator Module 4
FSB-FPGAs  PCIe-FPGAs  QPI-FPGAs  CPU DSP Libraries  ...

Intel Plan of Record

AAL Service API

**Physical Interconnect Protocol**

**System Memory**

**Physical Interconnect Protocol**

AFU: Acceleration Functional Unit
WS: Workspace in coherent, shared system memory

Under Investigation

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Backup
SARMTI POC Configurations

**Intel® SFC4UR “Foxcove” 4-processor system -- 4U Rack Mount Server**

- Four Intel Xeon® Processors L7345 (“Tigerton”) - 4 cores each @ 1.86 GHz; 8MB L2 cache 50W Max Thermal Design Power each
- Four Intel Xeon Processors MP X7460, 6 cores each @ 2.66 GHz, (“Dunnington’’); 16MB L3 cache. 130W Max Thermal Design Power
- 1066 MHz Front Side Bus
- 16 MB 667-MHz FBDIMMs
- Fedora* release 8 (Werewolf*) for x86_64 architecture (Linux* 2.6.23 kernel)
- Intel Math Kernel Library version 10.0

**Intel® SR1625 “Petrof Bay 2-processor server – 1U Rack Mount Server**

- 2 x Intel® Xeon Processors X5570 (“Nehalem-EP”) 4 cores each @ 2.93 GHz; QPI: 6.4 G transfers per second, 8M L2 Cache per processor 95W Max Thermal Design Power per processor
- 12 MB 1333MHz Registered ECC DDR3
- SCSI HARDDRIVE Seagate 146GB Savio 10k RPM SAS 2.5in SFF
- NUMA Optimized [Enabled] in BIOS
- Frequency scaling off: `/sbin/service cpuspeed stop`
- Centos 5.3 el5_x86_64 (RHEL) (Linux* 2.6.18 kernel)
- Intel Math Kernel Library version 10.2
- Intel Integrated Performance Primitives 6.1

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