FPGAs for IEEE Floating Point

FPGAs combine many of the features needed for high performance in numerical applications:
- High parallelism – hundreds of multipliers
- Massive memory bandwidth – hundreds of on-chip RAMs
- Moderate power consumption – 50% of Xeon, 25% of nVidia

New Altera compilation technology makes more floating point capability available.

High non-chip memory bandwidth keeps operands supplied.

Fused data paths reduce gate count and latency

Typical floating point block:
- Prenormalize operands
- Calculate
- Renormalize result,

Reducent normalization wastes gates and cycles.

Instead, consider each operation in the context of adjacent operations.
Guard bits eliminate need to post-normalize at every step.
Instead, worst-case analysis picks specific points for normalization.
Choose context-specific versions of each operator to minimize logic.

*Floating point data path synthesis for FPGAs,* Martin Langhammer, Proc. FPL 2008

On-chip bandwidth keeps pipeline full

B array: M9K
New column read from memories on every cycle: 16-128 DP values, (128-1K bytes).

A array: M144K
Multi-cycle read of row.
Row is re-used for multiple columns

Fused data path
Dot product for part of matrix multiply

Partial sum buffers

Fused data path
Final sum

Results

Floating Point performance:
47.46 Gflops IEEE double precision, until throttled by system bus!

No hard floating point cores
Achievable with standard parts

Sustained throughput
Major memories double-buffered