High-Performance, Parallel Embedded Architectures Using Acalis® CPU872 PowerPC® Multicore

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CPU Technology, Inc.

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Acalis Overview

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Acalis CPU872 Overview

- Secure Processor SoC containing 2 complete PPC compute nodes
- AT protection
- Supports Red/Black processing
- Protects software without degrading performance
- Highly efficient (MIPS/Watt)
- Balanced scalable performance (security, throughput, memory, I/O, communications, synchronization)
- Scalable without additional devices
- Industrial grade with minimum 10-year lifespan
### Acalis CPU872 Features & Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Security Functions</strong></td>
<td>- Scalable and programmable key structures</td>
</tr>
<tr>
<td></td>
<td>- Programmable On-chip Firewall</td>
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<td></td>
<td>- Anti-Tamper, Anti-Reverse Engineering</td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>- Up to 3.6G Operations (DMIPS, FLOPS)</td>
</tr>
<tr>
<td><strong>Typical Power</strong></td>
<td>- 8 Watts</td>
</tr>
<tr>
<td><strong>Process Technology</strong></td>
<td>- 90 nm CMOS (IBM Trusted Foundry)</td>
</tr>
<tr>
<td><strong>General Purpose Processors</strong></td>
<td>- Dual PowerPC® 440 Processor Cores</td>
</tr>
<tr>
<td></td>
<td>- Dual PowerPC Floating Point Units</td>
</tr>
<tr>
<td><strong>L1 Cache</strong></td>
<td>- 32KB data; 32KB instruction per PPC440 core</td>
</tr>
<tr>
<td><strong>L2 Cache</strong></td>
<td>- 256KB per PPC440 core</td>
</tr>
<tr>
<td><strong>Embedded DRAM</strong></td>
<td>- 4MB with ECC per PPC440 core</td>
</tr>
<tr>
<td><strong>Communication Processors</strong></td>
<td>- Dual Quintillium™ MPI Processors</td>
</tr>
<tr>
<td><strong>Streaming Processors</strong></td>
<td>- Dual Streaming Processors – 1024 Transactions</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>- 31 x 31 mm, 899-pin BGA package</td>
</tr>
</tbody>
</table>
## Acalis CPU872 Features & Specifications

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<thead>
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</tr>
</thead>
<tbody>
<tr>
<td>Inter-processor Interface</td>
<td>Five 10 Gbs Express interfaces</td>
</tr>
<tr>
<td>Ethernet Interface</td>
<td>10/100/1000 Ethernet controller</td>
</tr>
<tr>
<td>Serial Protocol Interfaces</td>
<td>Secure Boot Interface and I2C</td>
</tr>
<tr>
<td>Memory Controller to External DRAM</td>
<td>Dedicated 32/64-bit DDR2 with ECC per PPC440 Core</td>
</tr>
<tr>
<td>DMA Controller</td>
<td>Dual Multichannel with 64-bit addressing</td>
</tr>
<tr>
<td>Multiprocessor Interrupt Controller</td>
<td>One Universal Controller per PPC440 Core</td>
</tr>
<tr>
<td>Parallel Barrier Synchronization</td>
<td>Scalable to massive arrays</td>
</tr>
<tr>
<td>Mesh Router</td>
<td>64-bit Addressing</td>
</tr>
<tr>
<td>Programmable I/O Interface &amp; Timers</td>
<td>Industry Standard Interface</td>
</tr>
<tr>
<td>Software and Tools</td>
<td>Compatible with PowerPC-based operating environments</td>
</tr>
<tr>
<td>Availability</td>
<td>Samples Now to Qualified Customers</td>
</tr>
<tr>
<td></td>
<td>Production 4Q08</td>
</tr>
</tbody>
</table>

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Multi-Processor Benchmark Results

CPU872
Processor 0
Processor 1

CPU872
Processor 2
Processor 3

CPU872
Processor 4
Processor 5

CPU872
Processor 6
Processor 7

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Multi-Processor MPI Transfers

- Transfer $n$ bytes to processors on same chip, one-hop distance, and two-hop distance away

Start Timer
do {
    MPI_Send to X
    MPI_Recv from X
} 100 times
Stop Timer

- Elapsed time/200 = average one-way transfer time
Multi-Processor MPI Transfers

<table>
<thead>
<tr>
<th>Transfer Distance</th>
<th>Transfer Latency</th>
<th>Transfer Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8 Bytes</td>
<td>40 Bytes</td>
</tr>
<tr>
<td>On-chip</td>
<td>2.8 µs</td>
<td>3.8 µs</td>
</tr>
<tr>
<td>One-hop</td>
<td>3.9 µs</td>
<td>6.3 µs</td>
</tr>
<tr>
<td>Two-hop</td>
<td>4.8 µs</td>
<td>8.7 µs</td>
</tr>
</tbody>
</table>
Multi-Processor MPI Transfers

- Compare Latency*Power, Bandwidth/Power with other multiprocessors¹:
  - Acalis: 667 MHz PPC440, 8 W
  - MCR: 2.4 GHz Pentium Xeon, 65 W
  - ALC: 2.4 GHz Pentium Xeon, 65 W
  - Thunder: 1.4 GHz Itanium Tiger 4, 105 W
  - BlueGene/L: 700 MHz PPC440, 12 W (est.)

¹ (MPI at LLNL: MPI Performance Measurements, https://computing.llnl.gov/mpi/mpi_benchmarks.html)
Multi-Processor MPI Transfers

MPI Latency-Power Product, 40-Byte Transfers
(smaller is better)

Comparison of Latency * Power for different systems:
- Acalis
- MCR
- ALC
- Thunder
- BlueGene/L

Latency * Power (on-node) vs. Latency * Power (off-node)
Multi-Processor MPI Transfers

MPI Bandwidth-Power Quotient, 1024-Byte Transfers
(larger is better)
Multi-Processor Token Passing

- Single token passed around ring of processors, \( n \) times
- Each processor reads the token, increments it, passes token to next processor in the ring
- Measures finest practical parallel granularity.
Multi-Processor Token-Passing Code

```c
StreamingRegister * nextProcToken, * localToken;
long * localTokenValid, * nextTokenValid;
if (processor == 0) {
    *localToken = 0; *localTokenValid = 1;
} else *localTokenValid = 0;
forall processors {
    for (i = 0; i < n; i++) {
#ifdef MEMORY_TOKEN
    while (!*localTokenValid) ; *localTokenValid = 0;
    *nextProcToken = *localToken + 1; *nextTokenValid = 1;
#else
    *nextProcToken = *localToken + 1;
#endif
    }
    }
}
```
Token Passing Timing

- 667 MHz Clock, mix of on-chip and one-hop paths
- Memory-based token data and flag:
  - 552 ns to increment, pass a token (average)
  - Parallel grain size is 368 cycles of work (350-700 instruction-execution times)
- Streaming Register-based token:
  - 350 ns to increment, pass a token (average)
  - Parallel grain size is 233 cycles of work (220-450 instruction-execution times)
  - Communicate with other processors up to 2.8 million times/second without penalty
Pipelined Smith–Waterman Algorithm

- Smith-Waterman algorithm finds the best match of one string to another, assuming that characters may have been inserted, deleted, or substituted.
- Smith-Waterman algorithm can be applied to large classes of problems involving imperfect matching, including:
  - DNA similarity analysis, using an alphabet of 4 bases (Adenine, Cytosine, Guanine, Thymine)
  - Protein similarity analysis, using an alphabet of 20 amino acids
  - Plagiarism detection, using an alphabet of English words
Pipelined Smith–Waterman Algorithm

- Example: matching DNA string GCTGATATAGCT to DNA string GGGTGATTAGCT

- Similarity matrix defines scores for pairs of characters (eg. T-T = 1, C-G = -1)

- Penalties assigned for gaps (insertions/deletions)

- G C T G A T A T A G C T

- G G G T G A T A T A G C T
Pipelined Smith–Waterman Algorithm

- Smith-Waterman algorithm constructs a matrix of global similarity scores
- Algorithm run-time is quadratic in the lengths of the sequences
- Smallest human chromosome has over 1 million base-pairs
- Short DNA sequences (over 4000) each have 20-25 base-pairs
Pipelined Smith–Waterman Algorithm

- Large chromosome data distributed across all available processors
- Processors connected in a linear chain
- Short DNA sequences, similarity array data, best score data pipeline through chain of processors
- Program organized to allow load-time mapping of problem to available processors
Pipelined Smith–Waterman Results

Execution Times and Speedups for 1.1M Base-Pairs, 525 Short DNA Sequences

- Execution Time
- Speedup
- Execution time
- 23123/x

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Summary

• Acalis MPI hardware supports low latency-power product (< 120 us-W) and high bandwidth-power quotient (> 8 MB/sec/W) for inter-processor communication

• Acalis Streaming Registers provide low-latency communication to support medium-grained parallelism (< 500 instructions between synchronization)

• High-speed interconnects, on-chip and off-chip memories allow pipelined and parallel applications to run with minimal overhead (< 15%)
Summary

- High-performance secure processing COTS/NDI device for use in vital applications
- Industry-Leading Power / Performance Efficiency
- On-chip hardware Firewall, Anti-Tamper, and Anti-Reverse Engineering protects IP and sensitive data, without impacting performance
- Readily scalable from single chips to large arrays to meet any class of computing needs without additional logic
Acknowledgements
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